That which is claimed is:

1. A silicon carbide metal-oxide semiconductor field effect transistor unit cell, comprising:

an n-type silicon carbide drift layer;

a first p-type silicon carbide region adjacent the drift layer;

a first n-type silicon carbide region within the first p-type silicon carbide region;

an oxide layer on the drift layer, the first p-type silicon carbide region, and the first n-type silicon carbide region; and

an n-type silicon carbide limiting region disposed between the drift layer and a portion of the first p-type silicon carbide region, wherein the n-type limiting region has a carrier concentration that is greater than a carrier concentration of the drift layer.

2. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the portion of the first p-type silicon carbide region is adjacent a floor of the first p-type silicon carbide region.

3. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region is disposed adjacent a sidewall of the first p-type silicon carbide region.

4. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises a first portion disposed adjacent a floor of the first p-type silicon carbide region and a second portion disposed adjacent a sidewall of the first p-type silicon carbide region, and wherein the first portion has a carrier concentration greater than a carrier concentration of the second portion.

5. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the first p-type silicon carbide region is implanted with aluminum.

6. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising:

a gate contact on the oxide layer;

a source contact on the first n-type silicon carbide region; and

a drain contact on the drift layer opposite the oxide layer.

7. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises an epitaxial layer of silicon carbide on the n-type silicon carbide drift layer.

8. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 7, wherein the first p-type region is disposed in but not through the epitaxial layer of silicon carbide.

9. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region has a thickness of from about 0.5 μm to about 1.5 μm and a carrier concentration of from about $1x\ 10^{15}$ to about $5 \times 10^{17}\ cm^{-3}$.

10. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 6, wherein the gate contact comprises polysilicon or metal.

11. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising an n-type epitaxial layer on the first p-type silicon carbide region and a portion of the first n-type region, and disposed between the first n-type silicon carbide region and the first p-type silicon carbide region and the oxide layer.

12. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises an implanted n-type region in the drift layer.

13. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 6, further comprising an n-type silicon carbide substrate disposed between the drift layer and the drain contact.

14. A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising a second p-type silicon carbide region disposed within the first p-type silicon carbide region and adjacent the first n-type silicon carbide region.

15. A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide adjacent the drift layer;

a first region of n-type silicon carbide disposed between peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide within the first regions of p-type silicon carbide, wherein the second regions of n-type silicon carbide have a carrier concentration greater than a carrier concentration of the drift layer and are spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

an oxide layer on the drift layer, the first region of n-type silicon carbide and the second regions of n-type silicon carbide;

third regions of n-type silicon carbide disposed beneath the first regions of p-type silicon carbide and between the first regions of p-type silicon carbide and the drift layer, wherein the third regions of n-type silicon carbide have a carrier concentration greater than the carrier concentration of the drift layer;

source contacts on portions of the second regions of n-type silicon carbide;

a gate contact on the oxide layer; and

a drain contact on the drift layer opposite the oxide layer.

16. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide are adjacent the peripheral edges of the first regions of p-type silicon carbide.

17. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide and the third regions of n-type silicon carbide comprise an n-type silicon carbide epitaxial layer on the drift layer, and wherein the first regions of p-type silicon carbide are formed in the n-type silicon carbide epitaxial layer.

18. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide comprises a region of the drift layer.

19. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 18, wherein the third regions of n-type silicon carbide comprise implanted n-type regions in the drift layer.

20. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide has a higher carrier concentration than a carrier concentration of the drift layer and has a lower carrier concentration than a carrier concentration of the third regions of n-type silicon carbide.

21. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising an n-type epitaxial layer of silicon carbide on the first p-type regions and the first region of n-type silicon carbide.

22. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising an n-type silicon carbide layer between the drift layer and the drain contact, wherein the n-type silicon carbide layer has a higher carrier concentration than the carrier concentration of the drift layer.

23. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 22, wherein the n-type silicon carbide layer comprises an n-type silicon carbide substrate.

24. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising second p-type silicon carbide regions disposed within the first p-type silicon carbide regions.

25. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide have a thickness of from about 0.5 μm to about 1.5 μm.

26. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide have a carrier concentration of from about $1x\ 10^{15}$ to about 5×10^{17} cm^{-3}.

27. A silicon carbide metal-oxide semiconductor field effect transistor comprising:

an n-type silicon carbide drift layer;

spaced apart p-type silicon carbide well regions; and

an n-type silicon carbide limiting region disposed between the well regions and the drift layer.

28. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region is disposed between the spaced apart p-type well regions.

29. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region has a carrier concentration higher than a carrier concentration of the drift layer.

30. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region comprises an epitaxial layer of silicon carbide on the drift layer, and wherein the p-type well regions are disposed in but not through the epitaxial layer.

31. A method of fabricating a silicon carbide metal-oxide semiconductor field effect transistor unit cell comprising:

forming an n-type silicon carbide drift layer;

forming a first p-type silicon carbide region adjacent the drift layer;

forming a first n-type silicon carbide region within the first p-type silicon carbide region;

forming an oxide layer on the drift layer; and

forming an n-type silicon carbide limiting region between the drift layer and a portion of the first p-type silicon carbide region, wherein the n-type limiting region has a carrier concentration that is greater than a carrier concentration of the drift layer.

32. A method according to Claim 31, wherein the portion of the first p-type silicon carbide region is adjacent a floor of the first p-type silicon carbide region.

33. A method according to Claim 31, wherein forming an n-type limiting region further comprises forming the n-type limiting region adjacent a sidewall of the first p-type silicon carbide region.

34. A method according to Claim 31, wherein forming an n-type silicon carbide limiting region further comprises:

forming a first portion of the n-type silicon carbide limiting region adjacent a floor of the first p-type silicon carbide region; and

forming a second portion of n-type silicon carbide limiting region adjacent a sidewall of the first p-type silicon carbide region, wherein the first portion of the limiting region has a carrier concentration greater than the carrier concentration of a second portion of the limiting region.

35. A method according to Claim 31, wherein forming a first p-type silicon carbide region further comprises:

implanting aluminum in the p-type silicon carbide region; and

annealing the p-type silicon carbide region at a temperature of at least 1500°C.

36. A method according to Claim 31, further comprising:

forming a gate contact on the oxide layer;

forming a source contact on the first n-type silicon carbide region; and

forming a drain contact on the drift layer opposite the oxide layer.

37. A method according to Claim 31, wherein forming an n-type limiting region comprises:

forming an n-type epitaxial layer of silicon carbide on the n-type silicon carbide drift layer;

forming a mask on the epitaxial layer;

patterning the epitaxial layer to form the n-type limiting region.

38. A method according to Claim 37, wherein forming a first p-type region comprises forming the first p-type region in but not through the epitaxial layer of silicon carbide.

39. A method according to Claim 31, wherein forming an n-type limiting region comprises implanting n-type regions in the drift layer.

40. A method according to Claim 31, wherein the n-type limiting region is formed to a thickness of from about 0.5 μm to about 1.5 μm and a carrier concentration of from about 1×10^{15} to about 5×10^{17} cm^{-3}.

41. A method according to Claim 36, wherein the gate contact comprises polysilicon or metal.

42. A method according to Claim 31, further comprising forming an n-type epitaxial layer on the first p-type region and a portion of the first n-type region, and between the first n-type region and the first p-type region and the oxide layer.

43. A method according to Claim 36, further comprising forming an n-type silicon carbide substrate between the drift layer and the drain contact.

44. A method according to Claim 31, further comprising forming a second p-type silicon carbide region within the first p-type silicon carbide region and adjacent the first n-type silicon carbide region.

45. A method of fabricating a silicon carbide metal-oxide semiconductor field effect transistor, comprising the steps of:

forming a drift layer of n-type silicon carbide;

forming first regions of p-type silicon carbide adjacent the drift layer;

forming a first region of n-type silicon carbide between peripheral edges of the first regions of p-type silicon carbide;

forming second regions of n-type silicon carbide in the first regions of p-type silicon carbide, wherein the second regions of n-type silicon carbide have a carrier concentration greater than a carrier concentration of the drift layer and are spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

forming an oxide layer on the drift layer, the first region of n-type silicon carbide and the second regions of n-type silicon carbide; and

forming third regions of n-type silicon carbide between the first regions of p-type silicon carbide and the drift layer, wherein the third regions of n-type silicon carbide have a carrier concentration greater than the carrier concentration of the drift layer;

forming source contacts on portions of the second regions of n-type silicon carbide;

forming a gate contact on the oxide layer; and

forming a drain contact on the drift layer opposite the oxide layer.

46. A method according to Claim 45, wherein forming third regions of n-type silicon carbide further comprises forming the third regions of n-type silicon carbide adjacent the peripheral edges of the first regions of p-type silicon carbide.

47. A method according to Claim 45, further comprising forming an n-type silicon carbide epitaxial layer on the drift layer, wherein the first region of n-type silicon carbide and the third regions of n-type silicon carbide are formed from the epitaxial layer, and wherein the first regions of p-type silicon carbide are formed in the epitaxial layer.

48. A method according to Claim 45, wherein the first region of n-type silicon carbide comprises a region of the drift layer.

49. A method according to Claim 48, wherein forming third regions of n-type silicon carbide comprises forming the third regions of n-type silicon carbide by implanting n-type regions in the drift layer.

50. A method according to Claim 45, wherein the first region of n-type silicon carbide has a higher carrier concentration than a carrier concentration of the drift layer and has a lower carrier concentration than a carrier concentration of the third regions of n-type silicon carbide.

51. A method according to Claim 45, further comprising forming an n-type epitaxial layer of silicon carbide on the first p-type regions and the first region of n-type silicon carbide.

52. A method according to Claim 45, further comprising forming an n-type silicon carbide layer between the drift layer and the drain contact, wherein the n-type silicon carbide layer has a higher carrier concentration than the carrier concentration of the drift layer.

53. A method according to Claim 52, wherein the n-type silicon carbide layer comprises an n-type silicon carbide substrate.

54. A method according to Claim 45, further comprising forming second p-type silicon carbide regions within the first p-type silicon carbide regions.

55. A method according to Claim 45, wherein the third regions of n-type silicon carbide have a thickness of from about 0.5 μm to about 1.5 μm.

56. A method according to Claim 45, wherein the third regions of n-type silicon carbide have a carrier concentration of from about 1×10^{15} to about 5×10^{17} cm^{-3}.

57. A method of fabricating a silicon carbide metal-oxide semiconductor field effect transistor comprising:

forming an n-type silicon carbide drift layer;

forming spaced apart p-type silicon carbide well regions; and

forming an n-type silicon carbide limiting region between the well regions and the drift layer.

58. A method according to Claim 57, wherein forming an n-type silicon carbide limiting region further comprises forming the n-type limiting region between the spaced apart p-type well regions.

59. A method according to Claim 57, wherein the n-type limiting region has a carrier concentration higher than a carrier concentration of the drift layer.

60. A method according to Claim 57, wherein forming an n-type limiting region comprises forming an epitaxial layer of silicon carbide on the drift layer, and wherein forming spaced apart p-type well regions comprises forming spaced apart p-type well regions in but not through the epitaxial layer.